LogicFlex

User's Manual

LogicFlex User's Manual Version 1.3

Printed in U.S.A.
Document Part No. 94-0014
Published September 2002

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Overview

The LogicFlex single board computer is based on the Intel 386Ex microcomputer. The 386Ex is a high performance, 32-bit, single-chip microcomputer that is software compatible with the Intel 80386 family of microprocessors. Onboard Ethernet provides a direct connection to 10BASE-T networks. DOS compatibility allows development in a familiar environment with a wide range of tools. High endurance flash memory eliminates EPROM programming without worry of damaging the onboard non-volatile memory with repeated program cycles. Applications are uploaded directly into the flash disk. Expansion options provide high capacity flash storage eliminating the size and reliability problems associated with electro-mechanical storage devices.

Software development for the LogicFlex is remarkably simple and quick. Programs are written on a PC compatible computer in the language of your choice. After your application has been compiled or assembled and linked into .EXE or .COM form, it is uploaded to the LogicFlex's flash disk with your favorite telecommunications program using the X-Modem protocol. The application can then be tested and debugged through the console serial port. When the application is running to your satisfaction, the startup batch file can be modified so that the application will load and execute upon reset or powerup.

These features yield a quick and cost effective solution for applications such as networking, embedded web and serial protocol conversion.

Features

25MHz Intel 386Ex Processor
10BASE-T Ethernet Controller, NE2000 Compatible
5 Volt DC power
512k Bytes RAM Memory
512k Bytes Flash Memory
High Speed PC Compatible Serial Ports:
    1 Full-Function (8-wire) RS-232 Port
    1 Software Configurable as 3-wire RS-232 or RS-485
Synchronous 4-Wire Serial Port
3 PC Compatible Counter/Timers
Processor Watchdog (Generates Hardware Reset)
46 Digital I/O Lines
In-Circuit Programmable Xilinx CPLD (XC9572XL)
Hardware Clock/Calendar
LCD / Keypad Drivers
Processor Address/Data Expansion Bus
32Pin Dip Socket to accept 512k x 8 bit SRAM, 512k x 8 bit Flash, or
    M-Systems DiskOnChip 2000.
Support for Multi-I/O Expansion Boards
DOS and BIOS Compatible with the Flashlite386Ex and µFlashTCP
Compact Size, 4.20" x 3.60" (106.7 mm x 91.4 mm), 2.6oz (74 gm)

Operation

The LogicFlex is configured with two ‘disk drives’ A: and B:. Drive A: contains the operating system, the BIOS, and utility programs essential to the operation of the LogicFlex. Drive A: is read-only. Drive B: is read/write and contains optional utility programs and is available for user files and applications.

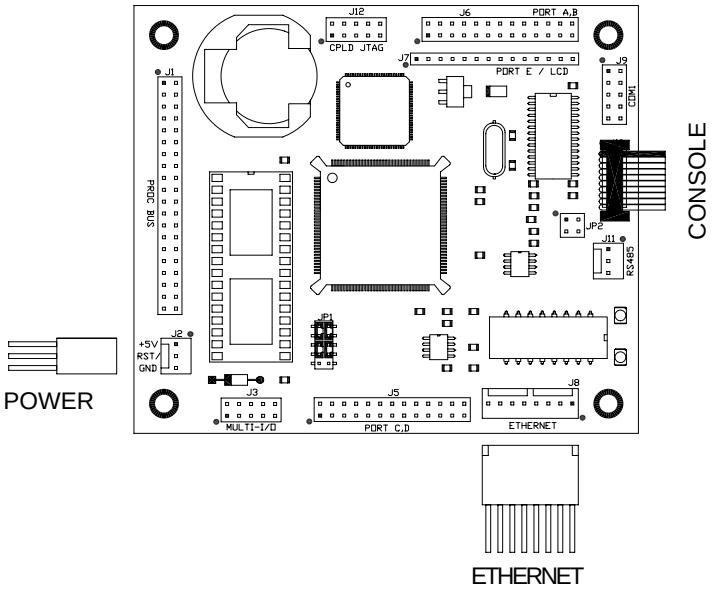
The serial port commonly known as COM2 on the PC is the console for the LogicFlex. The port is configured for 9600 baud, 8 data bits, 1 stop bit and no parity. This is the primary mode of communicating with the LogicFlex. DOS and the BIOS treat the console port as the logical devices STDIN and STDOUT. The second port is addressed and assigned interrupt vectors the same as COM1 on a PC. The console speed can be changed by reprogramming the COM2 baudrate divisor. See the LogicFlex webpage for more information.

When power is applied to the LogicFlex or when it is reset, the board goes through its initialization procedure and then starts DOS. A simple `AUTOEXEC.BAT` file is executed and then the board is ready to use. The batch file performs several functions before the user is given control. The DOS search path is set, the DOS prompt is set, the CTRL-C flag (discussed later in this manual) is checked and finally, an attempt is made to execute a file named STARTUP on the B: drive. This provides a convenient way for custom applications to execute immediately after initialization of the LogicFlex. If you wish to have your application start automatically, create a batch file named `STARTUP.BAT` that invokes the program. It is possible, but not recommended, to rename your application `STARTUP.EXE` or `STARTUP.COM`. If this is done and the program locks up, typing CNTL-C at bootup may not break the program and exit to the DOS prompt.

! Although the flash memory devices used have a guaranteed lifetime of over 10,000 write cycles, it is possible for an application to quickly wear them out. The flash memory is intended to store programs and setup data which is normally not changed. Avoid storing data or frequently changed information on the flash disk.

Getting Started

To begin development with the LogicFlex, you will need a PC compatible computer with a telecommunications program and a free serial port. Connect the LogicFlex's connector J10 to the PC's serial port with a 9-pin ribbon cable, PN 86-0000. Run the telecommunications program and configure the serial port for 9600 baud, 8 data bits, 1 stop bit, no parity, and no hardware flow control or software handshaking. Apply power to the LogicFlex, using our A/C adapter PN 88-0004 or a source of regulated 5V DC capable of supplying 400mA. J2 pin 1 (square pad on bottom of board) is positive.



The LogicFlex should respond with a welcome message and a B: prompt.

```
Bios Version 3.2l for Flashlite 386Ex with 256k or 512k Ram
DOS Version 3.3c for JK microsystems Flashlite
(C) HBS Corp and JK microsystems 1991-1999

B:\>
```

Enter `DIR` to look at the directory of drive B:. If you do not get a welcome message or echo of the characters that you type, you need to check your serial port setup. To test everything but the LogicFlex, remove the serial cable from J10 and jumper pins 3 and 5 with a wire or paper clip. If characters typed on the

keyboard are not echoed on the screen, the problem is with your setup. You must resolve the problem before you can continue.

If you were able to view the directory, take a few minutes to explore the contents of the LogicFlex's file system. You will find all of the essential utilities on drive A: and some optional programs on drive B:. Drive A: is write-protected and cannot be altered. Drive B: is read/write and can be changed or reformatted.

After you have looked at the programs on the LogicFlex, the next step is to try to upload a file. This is the procedure for getting files from your PC to the LogicFlex. On the LogicFlex, type the command `UP` followed by the name of the file you wish to upload. The LogicFlex will begin sending characters to your PC polling it for the file.

On your PC, start the transfer, usually by pressing the PgUp key. The telecomm program should respond by requesting the file name and protocol. Enter the file name and select X-Modem for the protocol. When the transfer is complete, you should get a new B: prompt on the screen. If the transfer does not work, the problem is most likely the Carrier Detect signal (pin 1 on the DB-9 connector) into the PC being sensed as low or false. Make sure that the signal is at least +3 volts into your PC if you are not able to transfer files.

If the transfer terminated without problems, you have a working development environment for the LogicFlex controller. At this point, you may wish to download the files `EDIT.COM` and `BASIC.COM` from the LogicFlex to your PC. Start the download on the LogicFlex by typing `DOWN BASIC.COM` and pressing Enter. On your PC, begin the transfer, usually by pressing PgDn. After the file is transferred, repeat the process with `EDIT.COM`. These files are also found on the JK microsystems web site.

The LogicFlex has a hardware clock calendar. When power is applied, DOS loads its clock from the hardware, and then maintains sepperate time/data information. When the time or date is set, DOS updates both its clock and the hardware clock. The time and date can be set with the following commands:

`B:\>TIME 13:30:00`	Sets the time to 1:30 pm
`B:\>DATE 6-19-2000`	Sets the date to June 19, 2000

The console output and input can be disabled on the LogicFlex with the `QUIET` and `NOQUIET` commands. This is useful for applications where both serial ports must communicate with hardware devices that would be disturbed by console messages. Before we look at the `QUIET` and `NOQUIET` commands, an overview of the LogicFlex boot procedure might be helpful.

When power is applied to the LogicFlex, one of the first things the BIOS initialization code does is check for a CNTL-C character typed at the console. If this character is typed as soon as the board is powered up or reset, a flag is set which overrides the quiet state of the console. The CNTL-C flag also prevents the BIOS from reading the hardware clock/calendar. When DOS runs its `AUTOEXEC.BAT` file on drive A:, the state of the CNTL-C flag is also checked and any user applications set to run on drive B: are not loaded. This insures that a hung application or quiet console can always be interrupted.

Running `QUIET` will turn off both input and output on the console port, allowing applications to use the hardware directly as COM2. Pressing CNTL-C immediately after reset or powerup will restore the console until the next reboot. Running `NOQUIET` will restore the default setting of an active console.

Some applications require switching console states on the fly. The quiet flag is stored in the flash BIOS and is copied to RAM when the board boots. Once in RAM, the flag is loacted at 40:008Bh and occupies the enitre byte. Writing a 0 to this location will enable the console, a 1 will disable the console. The C code below illustrates this process:

```
char far *c;
c=(char far *)MK_FP(0x40,0x8B);
*c = 0;                              /* turn on console */
*c = 1;                              /* turn off console */
```

If the CNTL-C flag is not set, the `AUTOEXEC` file will attempt to transfer control to a file named `STARTUP` on drive B:. DOS also looks for and, if present, loads `CONFIG.SYS` from drive B:.

A LogicFlex in quiet mode may appear to be non-functional. When troubleshooting a system, always try pressing CNTL-C while applying power.

Hardware

Memory Configuration

The 386Ex processor is initially configured in real mode with a physical address space of 1 megabyte. The SRAM is located between 00000h and 7FFFFh, the flash is between 80000h and FFFFFh. A 32-pin DIP socket is provided for additional flash, RAM, or EPROM data. This memory can be accessed by reprogramming the chip select unit in the 386Ex or by entering protected mode.

I/O Configuration

The 386Ex is configured for enhanced DOS mode. This mode provides access to the PC/AT peripherals such as UARTs, counter/timers, and the interrupt controller at their traditional I/O port addresses. Other 386Ex peripherals are accessible in expanded I/O space.

For addressing and programming the peripherals specific to the 386Ex, please refer to the Intel 386Ex Embedded Microprocessor User's Manual (Intel document number 272485-002). The manual is available in PDF format from our web site at http://www.jkmicro.com.

Digital I/O Ports

In its standard configuration, the LogicFlex has 7 ports controlling a total of 46 bits of I/O.

386Ex Port 1 bits 4,5,6 and 7, I/O Address F860 and F862 hex
These signals are available on J3. The data on Port 1 can be read from I/O address F860 hex. The default configuration is input. Each bit of Port 1 can be individually configured as an input or output. To configure a bit for output, write a zero in that bit position to I/O address F864 hex. To output data on Port 1, write the data to I/O address F862 hex.

P1PIN: F860h, Port Pin Status Register (read only), bits 4-7
P1LTC: F862h, Port Latch Register, bits 4-7
P1DIR: F864h, Port Direction Register, bits 4-7, 0 for output, 1 for input or open drain output.
P1CFG: F820h, Port Configuration Register, bits 4-7 low, route P1.4-P1.7 to chip pins (BIOS Default)

386Ex Port 3 bits 3 and 4, I/O Address F870 and F872 hex
Port 3 bits 3 and 4 are available on J3. The data on Port 3 can be read from I/O address F870 hex. The pins default to inputs. Each bit of Port 3 can be individually configured as an input or output. To configure a bit as an output, write a zero to that bit position in I/O address F874 hex. To output data on

Port 3, write the data to I/O address F872 hex. When used as inputs, these pins can also be configured to generate processor interrupts.

P3PIN: F870h, Port Pin Status Register (read only), bits 3-4
P3LTC: F872h, Port Latch Register, bits 3-4
P3DIR: F874h, Port Direction Register, bits 3-4, 0 for output, 1 for input or open drain output.
P3CFG: F824h, Port Configuration Register, bits 3-4 low, route P3.3-P3.4 to chip pins (BIOS Default)

Be careful to change only the required bits when working with the I/O ports. Pins on both ports 1 and 3 are used to control other on-board functions that can be reprogrammed or disabled through these configuration registers. See the Intel documentation for more information on configuring these ports.

Ports A - E, the remaining 40 bits of I/O, are controlled by a CPLD. The I/O from the CPLD is grouped into five 8-bit ports. Although the board ships with a standard program in the CPLD, the CPLD may be reprogrammed by the user. Information regarding designing with the CPLD is presented later in this manual. When using the factory programming, each of the five ports may be configured as either inputs or outputs. Additionally, when configured as inputs, ports A and B may be set to generate an interrupt if the state of any of that ports pins deviates from the value programmed to that ports comparison register. The following tables show the port registers, addresses, and configuration bits.

Register	Address
Port A	0x60
Port B	0x61
Port C	0x62
Port D	0x63
Port E	0x64
IOConf	0x65

Unlike Ports 1 and 3, Ports A through E have a single data register that is read/write. Data read from the port represents the current state of the port, data written to the port will be present on the port pins if the port is configured as an output. Each port may be configured as either an input or an output. Write a 0 to the appropriate bit in the direction register to configure the port as an input, write a 1 to configure it as an output. All ports default to inputs.

Port A and B can be configured to generate a processor interrupt if any of the pins of that port do not match that port's comparison register. The interrupt is enabled by writing a 1 to interrupt configuration bit for the desired port. The port must also have a 0 in its direction register. After the port is configured to

IO Configuration Register (I/O Port 65 hex)

Bit	7	6	5	4	3	2	1	0
Function	Not Used	Port B INT	Port A INT	Port E DIR	Port D DIR	Port C DIR	Port B DIR	Port A DIR
Default	1	0	0	0	0	0	0	0

generate interrupts, IRQ7/P3.5 is asserted when the current state of the input port deviates from the comparison value programmed for that port. The interrupt will remain asserted until a new value (matching the input state) is written to the comparison register or the input state changes to match the comparison register.

For example: To generate an interrupt whenever Port A deviates from hex 55, clear bit 0 of the configuration register (65 hex) to set the port direction as input. Write 55 hex to the PortA comparison register at 60 hex. Then set bit 5 of the configuration register (65 hex) to enable interrupts. An interrupt handler would also be installed to handle IRQ7. For more programming examples see the JK microsystems website or the LogicFlex development CDrom.

The CPLD is a low power device that operates from 3.3 Volts. Although the inputs are 5V complient, care must be taken to avoid exceding the current specifications for the device.

Programming the Ports

The I/O ports on the LogicFlex are mapped into the 386Ex I/O space. Using the ports with the C language requires the use of in and out functions unique to the x86 family of processors. Borland C functions `inport(`*`port`*`)` and `outport(`*`port,value`*`)`are 16 bit (word) instructions and `inportb(`*`port`*`)` and `outportb(`*`port,value`*`)` that are 8 bit (byte) instructions. These functions are part of the `dos.h` header file. Similar functions (and header files) are available for other C compilers and languages.

To access the I/O ports, the in and out functions must be used. Creating a pointer to the location may seem logical, but that reference would be in memory space, not I/O space. The following code illustrates the use of *inportb()* and *outportb()*.

```
unsigned char portA;
portA = inportb(PORT_DIR);      /* get value of dir. reg */
portA |= PORT_A_DIR_MASK;       /* set dir. bit for input */
outportb(PORT_DIR, portA);      /* write value to dir. reg */
printf("PORT A: %X\n", (int)inportb(PORT_A));
                                        /* read & print port A
value */
```

Asynchronous Serial (COM) Ports

The LogicFlex has 2 serial ports, COM1 and COM2. Both ports are internal to the 386Ex and are compatible with the 16450 UARTs on a PC. The maximum data rate is 115k Baud.

COM1 is wired as Data Terminal Equipment (DTE) for connection to a peripheral such as a modem. This is a full function RS-232 port implementing all of the handshaking and control lines with the exception of the Ring Indicator input. See Table 2h for the connector wiring. The UART base address is at I/O location 3F8h and can be configured to use IRQ 4.

COM2 is the default console and is wired as Data Communications Equipment (DCE) for direct connection to a computer or terminal. This port is software configurable as a 3 wire RS-232 port implementing RxD and TxD or as a half duplex RS-485 port. See Tables 2i and 2j for the connector wiring. The UART base address is at I/O location 2F8h and can be configured to use IRQ 3.

Table 1 shows the UART configuration and control registers. Please refer to the Intel 386Ex data sheet for more information on the serial ports and their configuration.

	7	6	5	4	3	2	1	0
Base	Receive/Transmit Holding Register / Divisor Latch Low (DATA)							
	Data In, Data Out							
Base+1	Interrupt Enable Register (IER)							
	0	0	0	0	Modem Status	Receive Line Status	Transmit Buffer Empty	Receive Buffer Full
Base+2	Interrupt Identification Register / Divisor Latch High (IIR)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Interrupt Source 00=Modem Status 01=Transmit Buffer Empty 10=Receive Buffer Full 11=Receiver Line Status		Interrupt Pending (0=Pending)
Base+3	Line Control Register (LCR)							
	Divisor Latch Access	Send Break	Parity 000=None, 001= Odd, 011=Even, 101=Mark, 111=Space			Stop Bits, 0=1, 1=2	Word Length, 00=5, 01=6, 10=7, 11=8	
Base+4	Modem Control Register (MCR)							
	0	0	0	Loop Back Test	Ext. Int. Enable	Out1	RTS	DTR
Base+5	Line Status Register (LSR)							
	Reserved	Transmit Register Empty	Transmit Buffer Empty	Break Interrupt	Framing Error	Parity Error	Overrun Error	Receive Buffer Full
Base+6	Modem Status Register (MSR)							
	DCD	RI	DSR	CTS	Δ DCD	Δ RI	Δ DSR	Δ CTS

Table1: UART Registers

The DATA and IER registers also hold the baud rate divisor. When the high bit of the LCR (DLA) is set, the divisor value can be written to DATA and IER. DATA contains the low byte and IER contains the high byte. To determine the divisor, divide 115200 by the required baud rate. Use a divisor with the nearest integer value. When access to the divisor value is no longer required, clear the DLA bit.

RS-485 Configuration

The COM2/Console port of the LogicFlex can be configured and used for RS-485 communications. In order to avoid conflicts with DOS and the BIOS, it is first necessary to move the console to COM1. This is done using the utility program `CON2COM1`. Please note that COM1 (J9) is pinned out as DTE and you must use a null modem cable to connect it to a PC serial port.

To enable RS-485 operation (and disable RS-232) on COM2, clear bit 6 of I/O port F872 hex.

```
#define EN485_MASK 0xBF
#define EN485_REG 0xF872
outportb(EN485_REG, (inportb(EN485_REG) & EN485_MASK) );
                                /* change to RS-485 */
```

Bit 0 of the PINCFG register must be set to allow control of the RS-485 transmit enable pin. The PINCFG register is located at I/O port F826 hex.

```
#define PINCFG 0xF826
outportb(PINCFG, (inportb(PINCFG) | 0x01) );
                                /* connect TE control to chip pkg
*/
```

The RTS line on COM2 is used to control the RS-485 transmitter. To transmit RS-485 data, set bit 1 of I/O port 2FC hex (mirrored at F8FC hex). To receive RS-485 data, clear bit 1. Note that the state of the chip pin is the inverse of the bit in the register (register=1, pin=0).

```
#define TX_MASK 0x02
#define TX_MASK_REG 0xF8FC
outportb(TX_MASK_REG, (inportb(TX_MASK_REG) | TX_MASK) );
                                /* enable transmitter */
outportb(TX_MASK_REG, (inportb(TX_MASK_REG) & ~TX_MASK) );
                                /* disable transmitter */
```

Two utility programs are available to aid RS-485 development. `485RX` accepts RS-485 data and displays it on the console. `485TX` accepts console data and sends it out the RS-485 port. The console must be set to COM1 when using these utilities. Both programs are installed on drive A:.

Watchdog Timer

The Watchdog Timer is a feature of the 386Ex processor chip. When in use, the watchdog counter decrements once per processor clock cycle. When the counter reaches zero, the WDTOUT pin is asserted for 8 processor clock cycles. This signal can be internally routed to IR7 or routed externally to generate a hardware reset. Software should periodically reload the counter register indicating that it is behaving properly.

The watchdog system has three modes: General Purpose, Software, and Bus Monitor. In General Purpose mode the counter can only be reloaded after it times out. This makes it difficult to use for system protection. The Software mode allows the countdown register to be reloaded before it times out. This allows protection against locked up software. The Bus Monitor mode is not applicable to the LogicFlex hardware.

To enable the watchdog in Software mode the following sequence must be followed:

1. Write the upper byte of the reload value to the WDTRLDH register (F4C0h)
2. Write the lower byte of the reload value to the WDTRLDL register (F4C2h)
3. Write two sequential words, F01Eh followed by 0FE1h, to the WDTCLR register (F4C8h)

Software will periodically repeat this sequence to refresh the counter and prevent it from generating an interrupt. The current value of the counter can be read from WDTCNTH and WDCNTL at F4C4h and F4C6h. Once enabled in Software mode, the timer can not be disabled.

The watchdog is active on power up, defaults to general purpose mode and the counter has an initial value of 3FFFFF hex. The counter can be disabled by setting bit zero of the WDTEN register at F4CAh. Please refer to the Intel 386EX Embedded Microprocessor User's Manual for more information.

Ethernet

The Ethernet port is a 16 bit design that supports direct connection to a 10BASE-T network, jumperless configuration, and NE2000 software compatibility. The controller has a default base address of 300 hex and IRQ9, using full duplex twisted pair wiring supporting link detection.

The Ethernet controller requires a software driver to interface with network software or other programs. The supplied packet driver (`NE2000.COM`) configures the chip interrupt, base address and other necessary parameters.

To install the packet driver, type:

```
B:\> NE2000 0x60
```

The parameter (0x60) is the software interrupt that programs will use to communicate with the driver. The number could be different, but 60h is common. The driver will install using the IRQ, I/O base address and MAC (Media Access Control) number stored in the on board configuration EEPROM. When the driver has loaded, it will indicate the system type, software interrupt, port address, IRQ, and MAC number (Ethernet Address). Note that hex values are preceded by '0x', consistent with C programming language syntax.

After the driver has been installed, network software will be able to communicate with the Ethernet adapter and the network. Users will probably want to modify their `STARTUP.BAT` file to automatically load the packet driver.

Other network drivers supporting NE2000 compatible hardware may be used. Drivers for software requiring NDIS or ODI support are available.

The board has two LEDs that indicated the status of the Ethernet link. The LNK LED indicates the status of the Ethernet. When illuminated, the LogicFlex is receiving the Ethernet 'heartbeat' and is connected to a live network. If this LED is not illuminated, there is a problem with the Ethernet wiring or the network. The ACT LED indicates activity on the network. The LED will flash when a data packet is received or transmitted.

Supported PC BIOS Functions

The Flashlite BIOS supports the following functions (software interrupts) common to PC compatible computers. Please refer to a DOS/PC reference for more information on DOS and BIOS software interrupts.

Int 10h, Video Driver, Functions 9 and Eh
Int 11h, Get Equipment Configuration
Int 12h, Get Memory Size
Int 13h, Disk Driver, Functions 0-4
Int 14h, Serial Port Driver, Functions 0-3
Int 16h, Keyboard Driver, Functions 0 and 1
Int 19h, Boot System
Int 1Ah, Real Time Clock Driver, Functions 0-5
Int 1Ch, Hook Timer Tick Interrupt
IRQ0, Timer Tick Interrupt

DiskOnChip 2000

M-Systems' DiskOnChip 2000 is a new generation of high performance single-chip Flash Disk. The DiskOnChip 2000 has become the standard Flash Disk module for Embedded Single Board Computers. The DiskOnChip MD2000 is a Flash Disk in a standard 32-pin DIP package that has built-in TrueFFS (True Flash File System) technology, allowing full read/write disk emulation. TrueFFS provides hard disk compatibility at both the sector and file level. Drives with capacities from 2 to 144 Mbytes are available. Drives larger than 32Mbyte require partitioning to allow XDOS to access the entire drive.

Install the DiskOnChip module in the memory expansion socket U10, noteing the location of pin 1. Set the Memory Type jumpers (JP1) for Flash memory. If the DiskOnChip is installed and functioning, there will be an installation message that is displayed during the boot process and a C: drive will be available to DOS.

```
Bios Version 3.2g for Flashlite 386Ex with 256k or 512k Ram
DOC Socket Services - Version 0.2
(C) Copyright 1992-1996, M-Systems Ltd.

TrueFFS-BIOS -- Version 3.3.7 for DiskOnChip 2000 (V1.10)
Copyright (C) M-Systems, 1992-1998

DOS Version 3.3c for JK microsystems Flashlite
(C) HBS Corp and JK microsystems 1991-1999

B:\>
```

Jumpers

JP1 - Socket Memory Type / Boot location

This jumper selects the type of memory in the expansion socket (U10) and which memory the board will boot from. Available choices are SRAM or Flash, onboard or expansion socket. Other memory types may be supported if their pinout is compatible with standard SRAM or Flash chips.
Jumper pins 1-2 and 3-4 for SRAM or pins 1-3 and 2-4 for Flash.
Jumper pins 5-7 and 6-8 to boot from the on-board memory or jumper pins 7-9 and 8-10 to boot from the expansion socket.
Default position: 1-3 and 2-4, Flash memory expansion.
5-7 and 6-8, Boot from on-board flash.

JP2 - RS485 Termination

This jumper enables or disables the termination and bias resistors used for the RS485 network. When the jumpers are installed on pins 1-2 and 3-4, the network is terminated with a 220 ohm resistance and biased to the space state. Remove the jumpers to disable termination.
Default position: 1-3 and 2-4, Termination enabled.

Cables and Connectors

The following tables show the connector pin and signal name (direction) for each pin.

NOTE: N/C indicates no connection and PULLUP indicates a 1k ohm pullup resistor to Vcc.
Outputs refer to signals driven by the board and received by a peripheral. Inputs are driven by a peripheral and received by the board.

COM1 is configured as a DTE port, and is generally used to communicate with a peripheral device. COM2 is configured as a DCE port, generally being used to connect the LogicFlex to another computer. A 10 pin dual row header to 9 pin D-type connector may be required to connect the expansion card to a peripheral or computer. See the tables below for connector pinouts.

The Ethernet port requires a short adapter (PN 86-0018) to connect between the 8 pin header (J8) and the RJ-45 style connector common to 10BASE-T networks. The default wiring for this adapter allows direct connection to a network hub with a straight through patch cord. If connection to a PC (without a hub) is required, the Tx and Rx pairs can be swapped. This can be accomplished by changing the adapter wiring as outlined below. If external LEDs for link and activity are required, they can be wired to pins 5 through 8 of J8. 680 ohm series resistors are provided on the PCB. Table 2g shows cable wiring and pin numbering information.

Pin 1 of a connector can be identified in several ways. Pin one has a square PCB pad and the others are round. This should be visible on the bottom of the PCB. Pin one will also be identified on the board silkscreen with a '1' and/or a dot. Dual row headers have ODD numbered pins on one side and EVEN numbered pins on the other. The dual row header numbering scheme follows the numbering for an IDC style ribbon cable. This numbering may not be identical to connectors with discrete wires. Use caution when connecting cables to the LogicFlex.

CPLD Programming

The LogicFlex design incorporates a Xilinx XC9572XL CPLD. In its default configuration, the CPLD is programmed with port I/O (PIO) logic as described earlier. If the end design requires different logic, the part may be reprogrammed via a JTAG interface.

Designing with CPLDs is a serious engineering task. This document does not cover PLD design. It is intended to help users get started with the LogicFlex and its capabilities. Users should exercise extreme care when creating a new logic design for the LogicFlex.

J1			Processor Bus
GND	1	2	VCC
GND	3	4	VCC
MREQ/	5	6	D7
MSTB/	7	8	D6
IOSTB/	9	10	D5
RW/	11	12	D4
REFRQ/	13	14	D3
RESET/	15	16	D2
IORD/	17	18	D1
IOWR/	19	20	D0
A9	21	22	A19/IRQ14
A8	23	24	A18/IRQ7
A7	25	26	A17/IRQ6
A6	27	28	A16/IRQ5
A5	29	30	A15
A4	31	32	A14
A3	33	34	A13
A2	35	36	A12
A1	37	38	A11
A0	39	40	A10

Table 2a: Processor Bus

J6			Port A & B
GND	1	2	3.3V
GND	3	4	3.3V
GND	5	6	SSTXCLK/
GND	7	8	SSRXCLK/
SSIORX/	9	10	SSIOTX/
PA.7	11	12	PB.7
PA.6	13	14	PB.6
PA.5	15	16	PB.5
PA.4	17	18	PB.4
PA.3	19	20	PB.3
PA.2	21	22	PB.2
PA.1	23	24	PB.1
PA.0	25	26	PB.0

Table 2b: Port A&B Pinout

J2	Power
+5V	1
RESET/	2
GND	3

Table 2c: Power Pinout

J3			Multi-I/O Bus
Data (P1.4)	1	2	CLK (P1.5)
Reset (P1.6)	3	4	CS (P1.7)
Vcc	5	6	GND
IRQ5 (P3.3)	7	8	IRQ6 (P3.4)
Vcc	9	10	GND

Table 2d: Multi-I/O Pinout

J12			CPLD JTAG
Vcc	1	2	TCK - IN
TDI - IN	3	4	TDO - OUT
TMS - IN	5	6	RESET
FLOAT/	7	8	GND
Vcc	9	10	GND

Table 2e: CPLD JTAG Pinout

J5			Port C & D
GND	1	2	3.3V
GND	3	4	3.3V
GND	5	6	3.3V
GCK2	7	8	GCK3
GOE1	9	10	GOE2
PC.7	11	12	PD.7
PC.6	13	14	PD.6
PC.5	15	16	PD.5
PC.4	17	18	PD.4
PC.3	19	20	PD.3
PC.2	21	22	PD.2
PC.1	23	24	PD.1
PC.0	25	26	PD.0

Table 2f: Port C&D Pinout

J8	Straight Through (to Hub)		LogicFlex Signal Name	Cross-Over (to PC)	
	RJ-45 Pin #	Color (86-0018)		RJ-45 Pin #	Color (86-0018)
1	1	BLU	TxD +	3	BLK
2	2	ORG	TxD -	6	YEL
3	3	BLK	RxD +	1	BLU
4	6	YEL	RxD -	2	ORG
5			LNK LED +		
6			LNK LED -		
7			ACT LED +		
8			ACT LED -		

Table 2g: Ethernet Pinout

Pin numbering on RJ45 cable plug

J9			COM1:
DCD (in)	1	2	DSR (in)
RxD (in)	3	4	RTS (out)
TxD (out)	5	6	CTS (in)
DTR (out)	7	8	N/C
GND	9	10	N/C

Table 2h: COM1 Pinout

J10			COM2:
PULLUP	1	2	N/C
TxD (out)	3	4	PULLUP
RxD (in)	5	6	PULLUP
N/C	7	8	PULLUP
GND	9	10	N/C

Table 2i: COM2 Pinout

J11	RS-485
DATA +	1
GND	2
DATA -	3

Table 2j: RS-485 Pinout

J7	Port E / LCD
GND	1
+5V	2
GND	3
RS / PE5	4
R/W / PE4	5
E1 / PE6	6
E2 / PE7	7
N/C	8
N/C	9
N/C	10
D4 / PE0	11
D5 / PE1	12
D6 / PE2	13
D7 / PE3	14

Table 2k: Port E Pinout

The CPLD is connected to the bus and its control lines. The remaining pins are routed to four connectors. The CPLD's JTAG programming pins are routed to both the 386Ex processor and to a connector. This scheme provides two methods of programming the CPLD in circuit. The device can be programmed, stand-alone, using a utility for the LogicFlex or with a PC using a Xilinx programming module (DLC4, DLC5 or equivalent).

Required Tools

The design process can be broken into several steps: logic design, design entry, fitting, simulation and programming. Software tools for most of these steps are available free from Xilinx (http://www.xilinx.com/sxpresso/webpack.htm). The WebPACK software has components for design entry, fitting and simulation. Xilinx and JK microsystems have utilities for programming the CPLD.

Logic Design

The majority of this step is left to the user, but there are a few key points that need to be addressed. Due to the nature of programmable devices there are an enormous number of ways to solve a problem and an equally large number of ways to get stuck.

The major area of concern is the processor bus. The CPLD is connected to the bus and its control lines. This necessary feature creates an easy way to design a non-functional LogicFlex. If the logic design of the CPLD does not allow the bus to operate in its intended manner, the LogicFlex will not function. Please review the appropriate section of the schematic and insure that the bus is treated properly. If for some reason the LogicFlex becomes non-functional after programming the CPLD, it will be necessary to reprogram it using another computer. Using Xilinx's cable and software, the chip can be erased or reprogrammed. This should return the LogicFlex to a functional state. When programming the CPLD from an external computer, it may be necessary to hold the LogicFlex in reset. This can be accomplished by tying pin 2 of J2 to ground (J2 pin 1) or pin 6 of J12 to Vcc (J12 pin 1 or 9). When using the Xilinx XChecker cable, attach the TDI, TCK, TMS, Vcc , and GND pins to LogicFlex with the flying leads. The TDO signal function will be performed by the XChecker signal labeled "RD". See Xilinx application note XAPP069 for more information.

Applications

The LogicFlex is compatible with a variety of interface drivers, TCP/IP stacks and network software. Discussion of the installation and operation of these packages is beyond the scope of this manual. Please refer to the software documentation or contact JK microsystems.

Care is required when setting up the LogicFlex on a network. Contact the Network Administrator if there are any questions about the required information. When working with a TCP/IP network, obtain the following information before starting your configuration: IP Address, Subnet mask, Name Server Address (DNS), and Gateway address. This information will be required during the configuration process. Other types of LANs require node names, workgroup names, etc. Proceed cautiously, networks can be easily disrupted when nodes are added without careful configuration.

Utilities

The LogicFlex comes preloaded with several utilities to aid system development. These utilities are located on drive A: of the LogicFlex or the Utilities disk.

UP.COM

This utility facilitates uploading files to the LogicFlex via the console port using the X-MODEM transfer protocol. The utility requires the user to supply the name of the incoming file. Unless otherwise specified, the file is placed in the active directory of the current drive. Be sure that B: is the current drive or a write-protect error will occur when UP tries to write to the read-only A: drive.

```
B:\>up

Upload file with X-MODEM Protocol
Usage:  up file...
Version 2.0 for JK microsystems Flashlite V25 and 386Ex

B:\>up test.exe

Ready, start X-modem upload now,
 Press CNTL-C to abort...
CCCC
B:\>
```

DOWN.COM

This utility facilitates downloading files from the LogicFlex via the console port using the X-MODEM transfer protocol. The utility requires the user to supply the name of the file to transmit.

```
B:\>down

Download file with X-MODEM Protocol
Usage:  down file...
Version 1.0 for JK microsystems SBC products

B:\>down test.exe

Ready, start X-modem download now,
B:\>
```

FORMAT.COM

If it becomes necessary to reformat the B: drive, FORMAT provides this function. CAUTION, all information on the drive will be lost during the formatting process.

```
B:\>format
Flashlite FLASH Drive Format Program -Version 3.0
System will reboot after successful format...

 Press 1 to initialize Drive B as 418 KB disk
 Press ESC to exit with no changes

>1
Flash Drive is now formatted
  Rebooting system...
```

EDIT.COM

A simple line editor is included to allow quick creation and modification of batch files or other text files. EDIT is similar to Microsoft's EDLIN provided in earlier versions of MS-DOS. It allows list, insert, delete, and modify. Upon exit, a backup of the original file is created (*filename*.BAK) and the edits are saved. If a backup file with the same name already exists, it is overwritten. A list of commands and their usage is available by entering 'h' at the edit prompt (>>). The name of the file to edit must be supplied following the command EDIT on the command line.

```
B:\>edit test.bat
FlashLite Line Editor v1.0
Enter h for help

New File: test.bat
>> i
       0: @echo Batch file being processed...
       1: mytsr
       2: myapp
       3: ^Z
>> l
       0: @echo Batch file being processed...
       1: mytsr
->     2: myapp

>> q
Save before exit (Y,n): y
File Saved
B:\>
```

DOS

JK microsystems' controllers use XDOS, a compact operating system for embedded applications. The XDOS command structure is nearly identical to MS/PC DOS version 3.3. The switches for the DIR command have been changed and expanded. XDOS does not support redirected input or output with the use of < and >, but does support pipes (|). None of the external DOS commands are available due to size constraints. XDOS does not support installable file system functions.

XDOS Command Reference

In the list below, XDOS commands are followed by a function description and their format including available parameters and switches. Items in boldface type must be entered. Capitals or lowercase letters may be used. Items in italics are parameters. Those in boldface italics must be entered, those in [ ] are optional. All switches are optional. They are shown as [/X]. Spaces and punctuation are to be included. An ellipsis ... following items means that you may repeat the items as often as needed. Do not enter the ellipsis or the square brackets. Most XDOS commands allow the use of wildcards in filenames and extensions. When wildcards (?=one character, *=any character or characters) are used, the command is executed once for each matching file.

Common parameters are:

[*d:*]	drive specification - a letter followed by a colon (:), e.g. A:, if no drive is specified, the default drive is used.
[*path*]	the path DOS must take in traveling from one directory to another; directory names are separated by a backslash (\).
[*filename*]	up to 8 characters used to name a file.
[*.ext*]	a three character extension may be added to a filename; an extension is separated from a filename by a period.

CD / CHDIR

Function:	Changes the current directory
Format:	**CD** or **CHDIR** [[*d:*]*path*]

COPY

Function:	Copies a file, combines two or more files into one file, or transfers data between files and DOS devices	
Format:	**COPY**	[*d:*][*path*]*filename*[*.ext*][*switches*] [+[*d:*][*path*]*filename*[*.ext*][*switches*] [*d:*][*path*][*filename*[*.ext*]][*switches*]
Switches:	/V - verify the contents of new file /A - copy file in ASCII format /B - copy file in binary format	

DATE

Function: Displays or changes the current DOS date.
Format: **DATE** [*mm-dd-yyyy*]

DEL / ERASE

Function: Deletes (erases) one or more files from a disk
Format: **DEL** or **ERASE** [*d:*][*path*][*filename*[*.ext*]]

DIR

Function: Lists directory entries
Format: **DIR** [*d:*][*path*][*filename*[*.ext*]][*switches*]
Switches: /a - display file attributes
/b - sort by file size (in bytes)
/d - sort entries by date and time
/f - display entries by alphabetic file name order
/n - display entries in directory order (do not sort)
/s - include system and hidden files in output
/h - display this Help screen (any invalid key)

MD / MKDIR

Function: Creates a subdirectory
Format: **MD** or **MKDIR** [*d:*]*path*

PATH

Function: Specifies directories that DOS is to search when trying to locate executable files
Format: **PATH** [[*d:*]*path*[;[*d:*]*path* ...]]

PROMPT

Function: Sets the DOS system prompt
Format: **PROMPT** [*text*]
Text: Resulting Character(s):

$t	The current time stored by DOS
$d	The current date stored by DOS
$p	The current directory
$v	The version of DOS being used
$n	The default drive
$g	The character >
$l	The character <
$b	The character |
$q	The character =
$$	The character $
$_	Carriage return plus line feed

REN

Function: Renames a file
Format: **REN** [*d:*][*path*]*filename*[*.ext*] *filename*[*.ext*]

RD / RMDIR

Function: Deletes a subdirectory
Format: **RD** or **RMDIR** [*d:*]*path*

TIME

Function: Displays or changes the current DOS time
Format: **TIME** [*hh:mm:ss.xx*]

TYPE

Function: Display the contents of a file
Format: **TYPE** [*d:*][*path*]*filename*[*.ext*]

VER

Function: Displays the DOS version number
Format: **VER**

VOL

Function: Displays the volume label of specified drive
Format: **VOL** [*d:*]

QuickBASIC Console I/O

Some of the code produced by Microsoft QuickBASIC and QuickBASIC Professional compilers does not execute properly on the LogicFlex. In the case of console I/O, we believe that QuickBASIC is generating code for specific hardware and software not present on the LogicFlex controller.

There are two problems with console I/O. The first is that a `PRINT` statement will not send output to the console port. To output text to the console, open "cons:" as a file and print to it. The second problem is that an `INPUT` statement will not echo the data entered by the user. To work around this problem, we have added a feature which allows the application to enable a console echo function in the BIOS. This feature is enabled by setting the byte at 40:8Ah to a one. Likewise, the local echo is disabled by setting 40:8Ah to a zero.

The following BASIC code demonstrates both of these workarounds:

```
start:
        OPEN "o", 1, "cons:"          ' console output
        PRINT #1, "What's your name? "' get string
        GOSUB echoOn                  ' turn on local echo
        INPUT name$                   ' get the name
        GOSUB echoOff                 ' turn off local echo
        PRINT #1, ""                  ' go down a line
        PRINT #1, "Hi , "; name$      ' print line and name
        END

echoOn:
        DEF SEG = &H40                ' BIOS data seg
        POKE &H8A, 1                  ' set local echo flag
        RETURN

echoOff:
        DEF SEG = &H40                ' BIOS data seg
        POKE &H8A, 0                  ' clear echo flag
        RETURN
```

Specifications

Supply Voltage:	5V ±5%
Supply Current:	400mA (nominal)
Operating Temperature:	-20 to +85 °C
Humidity:	5 - 90 % non-condensing

I/O Port Characteristics:

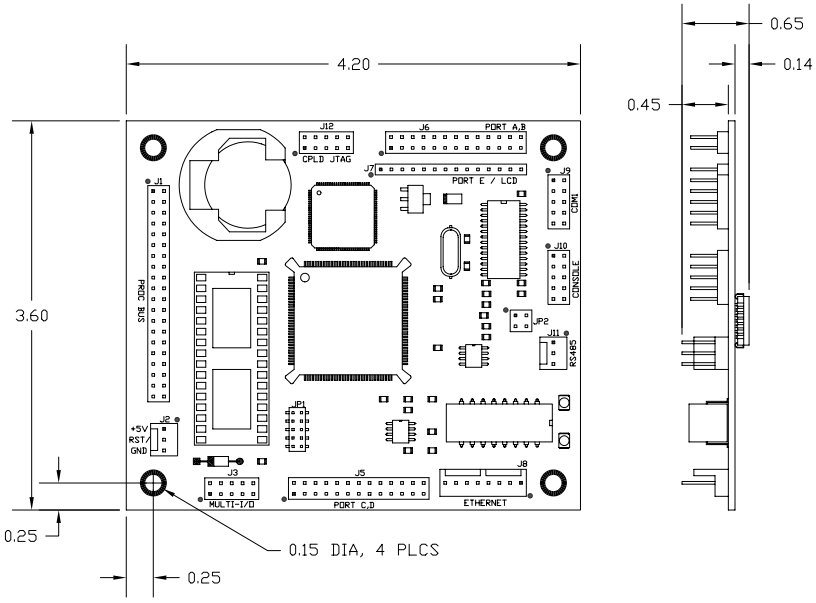
	Symbol	Parameter	MIN	MAX	Units	Condition
Port 1, 3:						
	V_{IL}	Input Low	-0.3	0.8	V	
	V_{IH}	Input High	2.0	Vcc+0.3	V	
	V_{OL}	Output Low		0.45	V	I_{OL}= 8mA
	V_{OH}	Output High	Vcc-0.5		V	I_{OH}= -8mA
Port A,B,C,D,E:						
	V_{IL}	Input Low	0	0.8	V	
	V_{IH}	Input High	2.0	5.5	V	
	V_{OL}	Output Low		0.4	V	I_{OL}= 8mA
	V_{OH}	Output High	2.4		V	I_{OH}= -4mA

Mating Connectors:

Connector	Mfg	MFG P/N	JK micro P/N
2x5 Housing			
J3, J9, J10, J12	Molex	22-55-2101	
	Oupiin	4072-2X05H	28-0030
2x13 Housing			
J5, J6	Molex	22-55-2261	
	Oupiin	4072-2X13H	28-0031
1x14 Housing			
J7	Molex	50-57-9014	
	Oupiin	4072-1X14H	28-0061
Pins			
	Molex	16-02-0096	
	Oupiin	404-PIN-10K	28-0033
1x3 Housing, Friction Lock			
J2, J11	Molex	22-01-2031	28-0012
1x8 Housing, Friction Lock			
J8	Molex	22-01-2081	28-0037
Pins, Friction Lock Housings			
	Molex	08-50-0114	28-0013

Mechanical:

Dimensions	4.20" x 3.60" (106.7 mm x 91.4 mm)
Weight	2.6oz (74 gm)



Rev	Date	Author	Changes
1.3	30SEP02	EW	Page 8, port 3 information was bits 0-5.
1.2	16APR02	EW	Fix Table 2k/J7 pinout: Pin4 was PE4, Pin 5 was PE5.
1.1	12SEP01	EW	Add change log Supply Voltage tollerance was +/- 10% Operating Temperature was -20 to 70 C

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