The LogicFlex-EPX packages a LogicFlex SBC and a comprehensive I/O board in a slim 1RU rack mount enclosure. I/O and power connections are made via 2-part, detachable screw terminals. Six push buttons and a 2x16 character LCD allow implementation of a user interface.

Features:

LogicFlex SBC:

- Intel 386Ex Processor, 25MHz
- 512K RAM / 512K Flash
- Ethernet, NE2000 compatible 10BASE-T
- Hardware Clock/Calendar
- Processor Watchdog (Generates Hardware Reset)
- Socket for Disk-On-Chip module

Digital Inputs:

- 16 Channels
- Configurable as Optically Isolated Voltage, Dry Contact, or TTL
- 2500 V Isolation (voltage or dry contact configuration)
- Voltage input: bi-directional (AC or DC), 5V < Vin < 48V

Relay Outputs:

- 16 Channels
- 125 VAC / 500mA Contacts
- SPDT Contact Configuration

User Interface:

- 6 Momentary push buttons
- 2 Line x 16 Character LCD with Backlight
- Ethernet Link and Activity LEDs

Power Supply / Connectors:

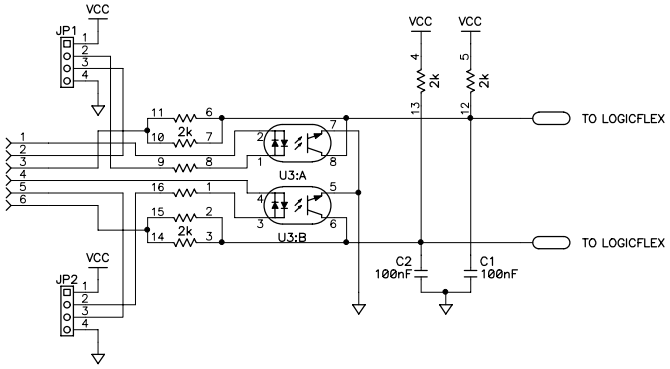
- Input Supply Voltage: 7-34 Volts DC
- Power: 5.5 W MAX
- I/O Connectors are 2-part plugable screw terminals
- RJ-45 Modular Connectors for Ethernet and Multi-I/O
- RJ-12 Modular Connectors for Serial Ports

Analog Inputs (optional):

- Maxim MAX197
- 8 Channel, 12 Bit Resolution
- 4 Software Programmable Input Ranges (0 to 5V, -5V to +5V, 0 to 10V, -10V to +10V)

Configuration:

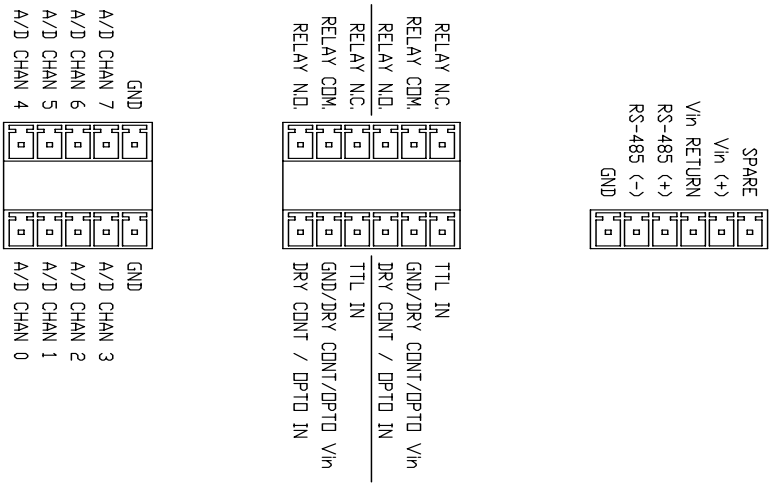
Jumpers JP1-JP16 configure the behavior of the opto-isolators on each input channel. The default setting jumpers pins 1-2 and 3-4 to yield an input to accept a dry contact closure between pins 1 and 2 of the input channel. Change the jumper to short pins 2-3 for a voltage input. The third input pin is connected to the LogicFlex processor board via a 1k series resistor, is pulled up with a 2k resistor and filtered with a 0.1µF capacitor. There is no additional protection on these input pin. The schematic below illustrates the input connections.



Connector Pinouts:

Inputs are connected to the lower half of the connector and outputs are connected to the upper half as illustrated below:

Connectors:



J1-J9 require 6 position pluggable terminal blocks (PCD # EVLP061G0, JK Part number: 28-0065)
J23 requires 5 position pluggable terminal blocks (PCD # EVLP051G0, JK Part number: 28-0076)

A/D Option:

The A/D option kit (JK part number 99-0057) consists of the Maxim A/D converter IC and the necessary connectors. Installing the A/D option is straight forward and only requires a #2 phillips screw driver. Remove the four screws that secure the top cover and open up the enclosure. Remove the three screws that hold the LogicFlex CPU card. Carefully remove the LogicFlex from the expansion board. Be careful not to bend the pins on the LogicFlex. Locate the empty 28pin dip socket. Insert the A/D converter IC in the socket being careful to orient the chip so that pin 1 is facing left (toward the 40pin bus connector). Also be sure that the chip pins install in the socket and are not bent. Reinstall the LogicFlex being sure that it is aligned properly with all of the sockets. Secure the LogicFlex and install the top cover.

Software:

`EXP_DRVR.OBJ` contains functions callable from C or QuickBASIC. This library allows easy access to the various I/O functions of the EPX board. The C and BASIC functions have common names and act identically. The assembly source code (`EXP_DRVR.ASM`) and C header file (`EPX_DRVR.H`) are also included. The object file may be regenerated using TASM. The distribution library has been compiled in the *large* memory model. If your project requires a *small* model library, the driver must be revised. Change the `largemodel` label to zero (0), and recompile the library.

All values passed and returned from the library functions are 16 bits wide. Many functions do not use all 16 bits, but the complete word is required. When the complete word is not used, data fills the low order bits and the high order bits are unused and ignored. In the following descriptions, C function syntax is shown first and BASIC syntax, where different, is shown in brackets ([ ]).

int GetVersion(*void*) [GetVersion(*data*)]

Returns the version number of the driver library.
Least significant digit is minor revision.
Most significant digits are major revision.

void InitIO(*void*)

Initialize EPX I/O. Initialize the Xilinx CPLD for use with the EPX board. Zero ports A and B and configure them as outputs. Increase 386Ex chip select 3 (*CS3) address range to include the A/D and front panel switch inputs.

void SetIOPt(*int address*)

Set (energize coil) specified OUTPUT
address refers to a relay channel. Address values range from 0 to 15

void ClrIOPt(*int address*)

Clear (de-energize coil) specified OUTPUT.
address refers to a relay channel. Address values range from 0 to 15

int GetIOPt(*int address*) [GetIOPt(*data*)]

Get state of specified INPUT. Returns 0 or 1.
address refers to an input channel. Address values range from 0 to 15

int GetSw(*int address*) [GetSw(*data*)]

Get specified Switch INPUT. Returns 0 or 1.
address refers to an input channel. Address values range from 0 to 7
Values 0-5 are the front panel pushbuttons, 6 is the A/D INT line, and 7 is 'SPARE' input (J9 pin 6).

void SetAD(*int value*)

Sets the input voltage range for subsequent conversions.
Specify a value from the following list:

0 = 0 to +5 volts
1 = 0 to +10 volts
2 = -5 volts to +5 volts
3 = -10 volts to +10 volts

int GetAD(*int channel*) [GetAD(*channel*)]

Returns the conversion results for the specified A/D channel.
channel refers to an input channel. Channel values range from 0 to 7.

A driver for the LCD, `LCD_LF.COM,` is installed on the LogicFlex. This driver emulates a line printer (stdprn) and greatly simplifies the process of displaying text on the LCD. `LCD_LF` is a TSR that is loaded before the user program. Characters written to STDPRN are redirected to the LCD. See the example programs for more details.

Revision	Date	Author	Changes
A	25 JULY 01	EW	First Issue